Page 2, please replace the ~~third~~ fourth paragraph with the following new paragraph:

For circuits that do not require high speed processing, occurrence of a no-patterned region can be avoided by lowering its integration degree. For circuits that require high speed processing, however, a higher integration degree (miniaturization) is needed, and in this case, design must be performed in preparation for occurrence of a no-patterned region. In addition, when a no-patterned region occurs, a problem of too much waste arises since the no-patterned region cannot be effectively utilized.

Page 2, please replace the fifth paragraph, continuing to page 3, with the following new paragraph:

In this manner, in a conventional LSI, since the minimum chip size is inevitably determined by the number and size of the input/output pads, a problem of a no-patterned region created in an active region surrounded by an I/O region arises in a highly integrated circuit or a circuit with a small number of gates. Thus, there are challenges of solving such a problem and improving the yield of a semiconductor device.

Page 3, please replace the second full paragraph with the following new paragraph:

In the semiconductor device thus configured, a no-patterned region having no circuit mounted therein is utilized in the active region where circuits can be mounted, and a plurality of logic circuits having functions identical to or different from those of logic circuits mounted in the remaining active region is mounted in the no-patterned region. Consequently, the device can be shipped as a product if at least one of the logic circuits operates normally to significantly improve and more effectively utilize the semiconductor device.

Page 4, please replace the seventh full paragraph, continuing to page 5, with the following new paragraph:

Arranged in the I/O region 12 are a plurality of input/output pads 14 which are electrodes for connecting lead-out terminals for a logic LSI with a circuit inside the semiconductor chip through bonding wire. Each of the input/output pads 14 is shaped to have a square with a side of approximately 100 μm.

Page 5, please replace the first full paragraph with the following new paragraph:

A hatched portion in Fig. 1 is a no-patterned region 13 where no circuit is mounted if only one logic circuit block is mounted in the active region 11 surrounded by the I/O region 12.

Page 5, please replace the third full paragraph with the following new paragraph:

As shown in Fig. 2, a portion of the no-patterned region shown in Fig. 1 is defined as a boundary region 15, and regions on both sides of the boundary region 15 are defined as a first active region 16 and a second active region 17, respectively. In the second active region 17, circuits having the same functions as, or circuits having different functions from, circuits mounted in the first active region 16, are mounted. It should be noted that the area of the first active region 16 may or may not be equal to the area of the second active region 17.

Page 7, please replace the fourth full paragraph, continuing to page 8, with the following new paragraph:

Conversely, when the signal SEL is set to HIGH level, since both the P-channel transistor T_{pa} and

A 9 (concluded)

N-channel transistor T_{na} are turned off, neither power nor ground is supplied to the block A and thus, the block A does not operate. However, since both the P-channel transistor T_{pb} and N-channel transistor T_{nb} are turned on, power and ground are supplied to the block B, and thus the circuits constituting the block B operate.

Page 10, please replace the sixth full paragraph, with the following new paragraph:

A 10

In addition, since a no-patterned region on a semiconductor chip can be considerably reduced to effectively utilize a semiconductor constituting a substrate, the utilization ratio for a wafer is significantly increased.

Page 12, please replace the first full paragraph with the following new paragraph:

A 11

To address this, since a no-patterned region is created with an increasingly miniaturized LSI in an active region where a circuit can be mounted, the present invention effectively utilizes such a region, which conventionally has been a no-patterned region, by mounting a redundant circuit there. Therefore, even when a portion of a logic circuit is defective, the redundant circuit is caused to function similarly thereto to allow improvement in the yield of the logic LSI.

IN THE CLAIMS:

Please enter the following amended claims:

Sub B1

A 12

1. (Amended) A semiconductor device, comprising

an I/O region formed on a chip and having at least an input/output pad;

a plurality of active region formed on said chip, said active regions being separated from one another by a boundary region;